

Performance Evaluation of wide Bandwidth RF Signal Generator Chip

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Abstract— The work in this paper is to give an overview of the compact wide band RF signal generator board design, emphasizing on the analyses and evaluation of the performance characteristics corresponding to the output signal purity and stability. The paper describes the design aspects involved in developing a reliable RF generating source which includes details regarding the factors that have taken care for optimum output power, spectral purity and noise performance. The simulation results obtained from the tool given by Maxim integrated are used as reference to evaluate the actual board when it is realised. These results are shown here for reference. Design aspects such as the power supply, noise filtering, loop filter component selection board layout consideration along with easy and compact form factor is considered. The board contains not only the signal generator device but also an FPGA from Xilinx to control the device, to make the board more useful for future applications; the board also has an SDRAM and an USB controller. This paper mainly concentrates on to MAX2870 signal generator and simulation results obtained by EE-Sim tool. Since the actual board is still in the process of being developed, the comparison of the actual performance to the simulation performance may not be possible at this point of time but definitely is in pipeline.

Keywords—FPGA, VCO, USB, SDRAM, PLL and DCM.

I. INTRODUCTION

Ultra wide band technology has been a very active field of research since last decade due to the advancements in IC technologies. Wide bandwidth signal generation has become a core part in communications, RADARs and high resolution sensor technologies. The challenge of integrating multiple modules to make signal generation systems more compact and reliable has been to an extent being addressed using the latest state of art synthesizer devices with integrated VCOs having reasonable spectral performance that is sufficient for number of applications. Analog devices, Hittite and Maxim are some of the leading IC manufacturers for synthesizer chips of similar kind. The recently released IC from Maxim is the

industry's only device which can output frequency from 25MHz to 6.0GHz while maintaining superior phase noise and spurious performance when combined with an external reference oscillator and loop filter. The high bandwidth requirements for systems such as Archaeological surveying instruments require multiple output matching stages which make it difficult for designer to design a system with constant pass band response along with high speed frequency hopping mechanisms.

High fabric frequencies with which FPGAs can be operated make a good choice for those to be used as a control and processing applications. Using FPGAs along with synthesizer allows us to configure the devices at high speeds so as to achieve large instantaneous bandwidth with good dwell time specifications.

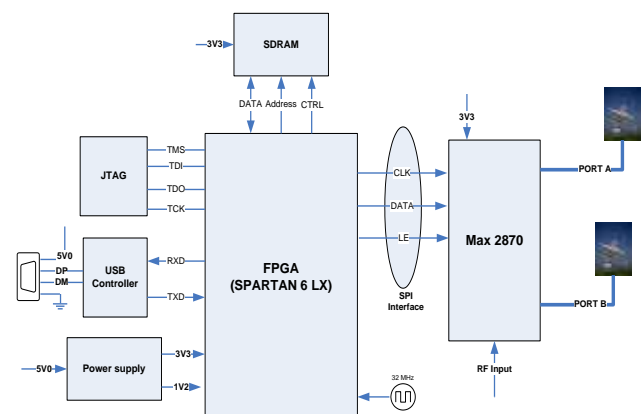


Fig. 1: Transmitter part of MAX2870 RF signal generator

II. THEORETICAL DETAILS

The Figure 1 shows the Transmitter part of RF signal generator which has Spartan 6 LX FPGA for controlling the MAX2870 synthesizer through SPI interfaces. The FPGA has approximately 50 I/O lines. The block diagram also shows a dual channel USB, integrated JTAG programmer, 128Mb SDRAM, efficient switching power supply and MAX2870 synthesizer [7]. The MAX2870 is an ultra-wideband phase-locked loop (PLL) with integrated Voltage Control Oscillators (VCOs) capable of synthesizing frequencies from 25MHz to 6.0GHz while

maintaining superior phase noise and spurious performance when combined with an external reference oscillator and loop filter. The MAX2870 is a high-performance frequency synthesizer [1]. The ultra-wide frequency range is achieved with the help of multiple integrated VCOs covering 3000MHz to 6000MHz, and output dividers ranging from 1 to 128. The device also provides dual differential output drivers, which can be independently programmable to deliver -4dBm to +5dBm output power. Both outputs can be muted by either software or hardware control [1].

Comparison was made between MAX 2870 and ADF4350 Synthesizers. The MAX device was chosen for the applications because of the advantages over other synthesizers in terms of the MAX2870 provide an additional method to switch between integer and fractional modes. The MAX2870 provides a 16-bit resolution with an extended usable range; The MAX2870 provides programmability on the CP output clamp to achieve better noise performance in integer-N mode. The MAX2870 allows the user to disable the VCO auto selection (VAS) machine, and manually set the VCO sub band. Using a VCO lookup table, the user can achieve a faster PLL lock time than with the VAS enabled [8].

The Spartan 6 offers the more flexible CMT which allows 36Kbit BRAM blocks to be split into two 9Kbit BRAM blocks. It also provides DCMs and PLLs [7]. The Spartan 6 has more built-in SRAM - 64Kbytes [7].

The PCB is a four layer, independent analog and digital ground separation design, for the in-built ADC in the MAX2870. The differential clock outputs are maintained to avoid noise injection through the track. The ground layered is sandwiched between the signal layer as the TOP layer and the Power layer at the BOTTOM.

III. EXPERIMENT AND SIMULATION

The first paragraph under each heading or subheading should be flush left, and subsequent paragraphs should have a five-space indentation. A colon is inserted before an equation is presented, but there is no punctuation following the equation. All equations are numbered and referred to in the text solely by a number enclosed in a round bracket (i.e., (3) reads as "equation 3"). Ensure that any miscellaneous numbering system you use in your paper cannot be confused with a reference [4] or an equation (3) designation.

The MAX2870 is controlled by a 3-wire serial interface and is compatible with 1.8V control logic. Maxim integrated has a tool to simulate the design parameters. When design requirements are entered in the EE-sim tool, the interactive schematic and bill of materials are generated and can be used for evaluating the design. In this paper the tool is used for evaluating the theoretical

part of the design and the board is generated to evaluate the design with practical output [7].

The design parameters that were considered for the simulations are:

Output Frequency: 4.5GHz

Rset: 5.1K Ω

Charge Pump Current (I_{cp}): 0.32mA

Reference Multiplier: x1

Reference Divider: 2

Reference Frequency: 50MHz

Loop Filter Design Specifications:

Desired PLL Loop Bandwidth: 50 kHz

Desired Phase Margin: 50

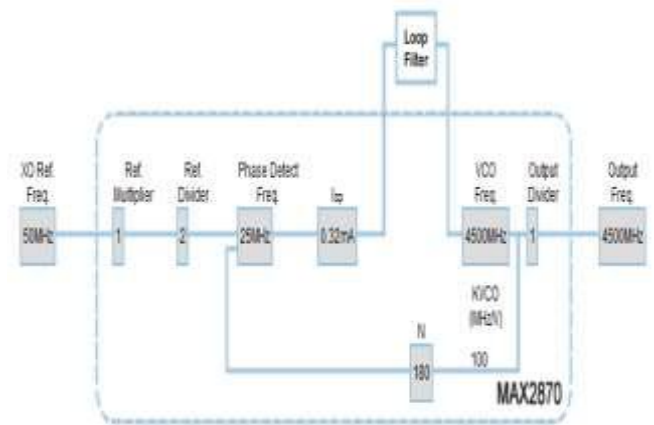


Fig. 2: PLL configuration [6]

When above configuration parameters are fed to the EE-Sim tool of Maxim integrated, the configuration block diagram was generated and is shown in Figure 2

The design parameters can also be modified using the EE-sim tool for designing to different frequencies. The parameters that can be varied to get different frequencies are allowed to modify in the EE-sim tool.

The design performance has been investigated through simulation via EE-sim tool of maxim integrated. The results are captured for various parameters and the simulations are done for 4.5GHz centre frequency. Presently the board is being developed as per the block diagram shown in Figure 1 and also, parallel to board design the component procurement and the simulation of the MAX2870 device is also being conducted. Once the fabricated board arrives and the components are assembled; then the simulated results are evaluated with the practical outputs.

The registry update rate of MAX2870 device compared with other synthesizer device available from analog devices is of the value is 8 nS approximately which could lead to slew rate of less than 2 nS at the control signal clock. There has to be ground stitching around the critical traces which are required to be isolated through low power RF signals.

Some of the major factors that has to be considered for step frequency synthesizer is the hop signal time and the locking period required by the device, this requires operational calculation for getting the designed loop bandwidth and phase margin (Figure 5) so as to achieve step of 1 MHz instantaneous with in dwell time of one millisecond.

The overall integrated phase noise (Figure 6) could be judged based on the noise floor of the external clock signal, the loop bandwidth and internal VCO characteristics which intern also be effected by the jitter on control signal.

The various simulation results are captured in Figure 3, Figure 3, Figure 4 and Figure 5.

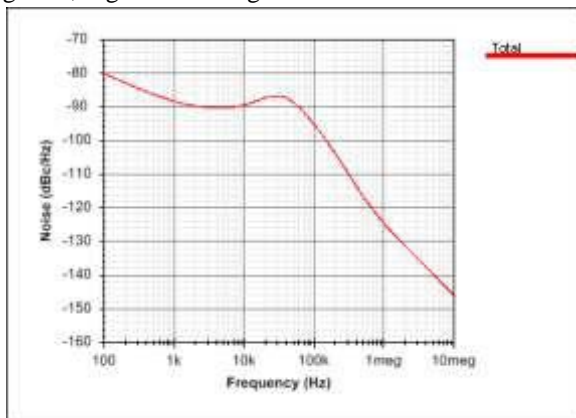


Fig. 3: Noise Total

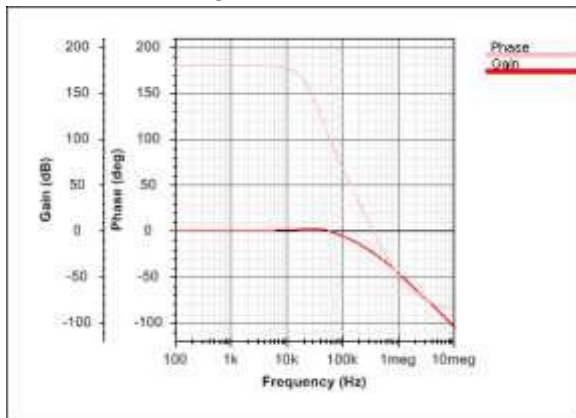


Fig. 4: Closed Loop Gain/Phase Margin

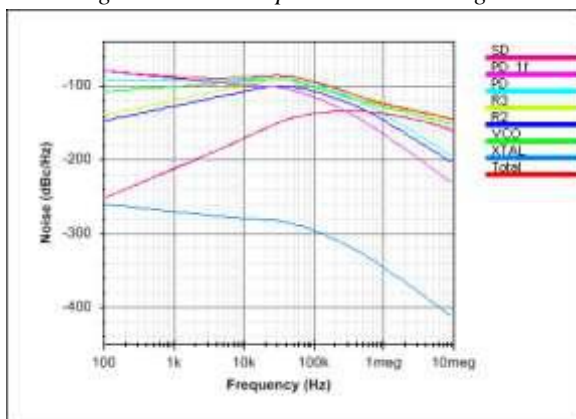


Fig. 5: Noise Total (w/ Component Curves)

IV. RESULTS AND DISCUSSION

The digital circuit has the switching regulator which generate noisy digital signal that could affect noise floor of the system. High-Q dc line filter has to be implemented at the output of regulator in the digital section and add ferrite beads at all significant power supply lines given to the synthesizer chip and associated circuitry. Snap shot of the schematics of the board that is being developed is shown in Figure 8. ORCAD is the tool used for generating the schematics.

The power supply circuit that is required to drive the board is designed using Linear Technologies step down regulator. The Figure 7 shows the snapshot captured in orcad. The input voltage range is 2.5V to 5.5V, making it ideal for USB powered applications. Supply current during operation is only 35μA and drops to <1μA in shutdown. A user-selectable mode input allows the user to trade-off between high efficiency Burst Mode operation and pulse-skipping mode. An internally set 2.25MHz switching frequency allows the use of tiny surface mount inductors and capacitors. Internal soft-start reduces inrush current during start-up. Both outputs are internally compensated to work with ceramic output capacitors.

One of the most important things to be taken care for generating clean spectral output is to see that the loop filter does not induce coupling due to the nearby high speed signals on the board. This could act as modulation signal to the output if loop filter section is not properly isolated. The output trace has to be matched for wide band so as to keep VSWR constant throughout the desired band within the acceptable limit. The input clock has to be fed directly to synthesizer chip to avoid any phase noise degradation.

The MAX2870 serial interface contains five write-only and one read-only 32-bit registers. The 29 most-significant bits (MSBs) are data, and the three least-significant bits (LSBs) are the register address. Register data is loaded MSB first through the 4-wire serial interface (SPI). When LE is logic-low, the logic level at DATA is shifted at the rising edge of CLK. At the rising edge of LE, the 29 data bits are latched into the register selected by the address bits. The user must program all register values after power-up [7].

The MAX2870 can be put into low-power mode by setting SHDN = 1 or by setting the CE pin to logic-low [7].

The device has dual differential open-collector RF out-puts that require an external RF choke 50 ohm resistor to supply for each output. Each differential output can be independently enabled or disabled by setting bits RFA_EN and RFB_EN. Both outputs are also controlled

by applying a logic-high (enabled) or logic-low (disabled) to pin RFOUT_EN [7].

The output power of each output can be individually controlled with APWR for RFOUTA and BPWR for RFOUTB. The available differential output power settings are from -4dBm to +5dBm, in 3dB steps with 50 Ω pull-up to supply. The available single-ended output power ranges from -4dBm to +5dBm in 3dB steps with a RF choke to supply. Across the entire frequency range different pull-up elements (L or R) are required for optimal output power. If the output is used single ended, the unused output should be terminated in a corresponding load [7].

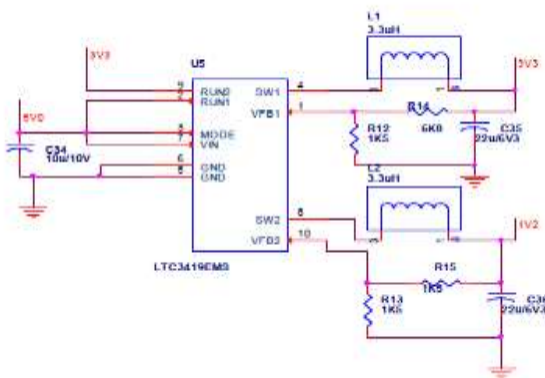


Fig. 6: Schematic of power supply circuit

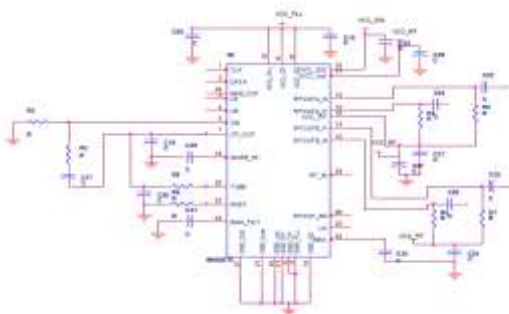


Fig. 7: Schematic of Max2870 captured using ORCAD tool

VCO: The fundamental VCO frequency of the device guarantees gap-free coverage from 3.0GHz to 6.0GHz using four individual VCO core blocks with 16 sub-bands within each block. Connect the output of the loop filter to the TUNE input. The TUNE input is used to control the VCO [7].

V. CONCLUSION FUTURE WORK

This paper provides simulation results from the tool that are used to derive the output performance of device in ideal conditions based on the system requirements and design features described error margin will be tested on the practical board. One channel of this transmitter board

will be used to provide the local oscillator frequency to the base band conversion receiver as well, which will provide more accurate phase locked source as the lag between transmitted source and the receiver reference source will be same. The work is still pending on developing a SDRAM controller and USB controller inside FPGA. The reason for developing a board is to use the synthesizer output at the antenna for transmitting as well as for receiving the signals from the antenna and sampling them. Antenna design work is in preliminary stages and yet to decide the type of antenna [9] along with the specs that is to be used.

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